Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of fabricating a semiconductor device, the method comprising:

measuring a patterned gate length of a patterned gate structure, wherein measuring the patterned gate length comprises measuring a dimension of a patterned test structure in a scribe line region of a wafer;

forming offset spacers along sides of the patterned gate structure, wherein a width of the offset spacers is determined according to the patterned gate length; and

implanting drain extension regions of a semiconductor body after forming the offset spacers.

2. (Original) The method of claim 1, wherein forming the offset spacers comprises:

conformally depositing an offset spacer material layer over the top and sides of the patterned gate structure and above prospective source/drain regions of the semiconductor body; and

performing an anisotropic etch process that removes portions of the offset spacer material from prospective drain extension regions of the semiconductor body and leaves offset spacer material along the sides of the patterned gate structure.

3. (Original) The method of claim 2, wherein the offset spacer material comprises silicon nitride or silicon oxide.

4. (Original) The method of claim 2, wherein the offset spacer material comprises silicon nitride, further comprising forming an oxide over the patterned gate

structure and over the prospective drain extension regions of the semiconductor body prior to conformally depositing the offset spacer material layer.

5. (Original) The method of claim 2, wherein the offset spacer material layer is deposited to a thickness determined according to the patterned gate length.

6. (Original) The method of claim 5, wherein the thickness of the deposited spacer material is about half the difference between a constant and the measured patterned gate length.

7. (Original) The method of claim 6, wherein the constant is related to a desired channel length.

8. (Original) The method of claim 5, wherein the anisotropic etch process is controlled according to the measured patterned gate length.

9. (Original) The method of claim 8, wherein the thickness of the deposited spacer material and the anisotropic etch process are controlled so that the width of the offset spacers is about half the difference between a constant and the measured patterned gate length.

10. (Original) The method of claim 9, wherein the constant is related to a desired channel length.

11. (Original) The method of claim 2, wherein the anisotropic etch process is controlled according to the measured patterned gate length.

12. (Original) The method of claim 11, wherein the anisotropic etch process is controlled so that the width of the offset spacers is about half the difference between a constant and the measured patterned gate length.

13. (Original) The method of claim 12, wherein the constant is related to a desired channel length.

14. (Original) The method of claim 2, wherein the thickness of the deposited spacer material and the anisotropic etch process are controlled so that the width of the offset spacers is about half the difference between a constant and the measured patterned gate length.

15. (Original) The method of claim 14, wherein the constant is related to a desired channel length.

16. (Original) The method of claim 1, wherein the width of the offset spacers is about half the difference between a constant and the measured patterned gate length.

17. (Original) The method of claim 16, wherein the constant is related to a desired channel length.

18. (Original) The method of claim 1, wherein the offset spacers comprise silicon nitride or silicon oxide.

19. (Original) The method of claim 1, wherein measuring the patterned gate length comprises one of scanning electron microscopy, atomic force microscopy, and scatterometry.

20-26. (Cancelled) The method of claim 1, wherein measuring the patterned gate length comprises measuring a dimension of a patterned test structure in a scribe line region of a wafer.